Amendments to the Claims:

Please cancel claims 1-30.

This listing of claims will replace all prior versions, and listings, of the claims in the application:

Listing of Claims:

1-30 (Canceled)

31. (Original) A process for fabricating two memory levels in a memory array comprising:

forming a first conductive layer;

depositing a first semiconductor layer over the first conductive layer, the first semiconductive layer being doped with a first conductivity type dopant;

etching the first conductive layer and the first semiconductor layer into a plurality of first parallel, spaced-apart rail-stacks;

filling the space between the first rail-stacks with a first insulator;

planarizing the first upper surface of the first rail-stacks and the first insulator;

forming a first antifuse layer over the planarized first upper surface;

depositing a second semiconductor layer doped with a second conductivity type dopant over the first antifuse layer;

forming a second conductive layer over the second semiconductor layer;

depositing a third semiconductor layer doped with a second conductivity type dopant over the second conductive layer;

etching the second semiconductor layer, second conductive layer, and third semiconductor layer into a plurality of second parallel, spaced-apart rail-stacks;

filling the space between the second rail-stacks with a second insulator;

planarizing the second upper surface of the second insulator and the second rail-stacks;

forming a second antifuse layer on the planarized second upper surface;

depositing a fourth semiconductor layer doped with a first conductivity type dopant over the second antifuse layer;

forming a third conductive layer;

etching the third semiconductor layer and third conductive layer to form third parallel, spaced-apart rail-stacks;

filling the space between the third rail-stacks with a third insulator.

32. (Original) The process defined by claim 31, wherein the first, second, third, and fourth semiconductor layers comprise polysilicon layers.

33. (Original) The process defined by claim 31, wherein the first conductivity type is N type, and the second conductivity type is P type.

34. (Original) The process defined by claim 33, wherein the N type polysilicon layers are doped to a concentration level of N-, and the P type polysilicon layers are doped to a concentration level of P+.

35. (Original) The process defined by claim 31, wherein the first and second antifuse layers comprise silicon dioxide.

36. (Original) The process defined by claim 31, wherein the first, second, and third rail-stacks have approximately the same height.

37. (Original) The process defined by claim 31, wherein the first, second, and third conductive layers comprise a silicide.

38. (Original) The process defined by claim 37, wherein silicon is deposited on a metal layer to form the silicide.

39. (Original) A process for fabricating two memory levels in a memory array comprising:

forming a first conductive layer;

depositing a first semiconductor layer over the first conductive layer, the first semiconductive layer being doped with a first conductivity type dopant;

etching the first conductive layer and the first semiconductor layer into a plurality of first parallel, spaced-apart rail-stacks;

filling the space between the first rail-stacks with a first insulator;

planerizing the first upper surface of the first rail-stacks and the first insulator;

forming a first antifuse layer over the planarized first upper surface;

depositing a second semiconductor layer doped with a second conductivity type dopant over the first antifuse layer;

forming a second conductive layer over the second semiconductor layer;

depositing a third semiconductor layer doped with a second conductivity type dopant over the second conductive layer;

depositing a fourth semiconductor layer doped with a first conductivity type dopant over the third semiconductor layer;

etching the second semiconductor layer, second conductive layer, third semiconductor layer and fourth semiconductor layer into a plurality of second parallel, spaced-apart rail-stacks and an etched fourth semiconductor layer;

filling the space between the second rail-stacks and the etched fourth semiconductor layer with a second insulator;

planerizing the second upper surface of the second insulator and the etched fourth semiconductor layer;

forming a second antifuse layer on the planarized second upper surface;

forming a third conductive layer;

etching the third conductive layer and etched fourth semiconductor layer to form third parallel, spaced-apart rail-stacks;

filling the space between the third rail-stacks with a third insulator.

40. (Original) The process defined by claim 39, wherein the first, second, third, and fourth semiconductor layers comprise polysilicon layers.